

CLAIMS

What is claimed is:

1. A method of forming a P-N junction within a semiconductor substrate, comprising:

forming a coating comprising a dopant over a surface of the semiconductor substrate; and

5 heating the semiconductor substrate to cause a portion of the dopant to diffuse from the coating into the semiconductor substrate and thereby form a P-N junction within the semiconductor substrate;

wherein the semiconductor substrate comprises a single crystal;

10 prior to heating, the single crystal comprises a semiconductor that forms the majority of the crystal and an impurity atom that forms a part of the crystal and is distributed primarily within a layer of the crystal adjacent the surface;

the impurity atom has a dose of at least about 1×10^{13} atoms/cm² within the layer;

15 the semiconductor has an interstitial form; and

at 1000 °C, the impurity atom is a faster diffusing species relative to silicon atoms.

2. The method of claim 1, wherein prior to heating, the impurity atom
20 has a dose of at least about 1×10^{14} atoms/cm² within the layer.

3. The method of claim 1, wherein the impurity atom is fluorine.

4. The method of claim 1, wherein after heating 90% of that portion of
25 the dopant that has diffused into the semiconductor substrate is located within about 50 nm of the surface.

5. The method of claim 1, wherein the dopant is boron.

6. The method of claim 1, wherein after heating the concentration of the dopant within the substrate adjacent the surface is at least about 1×10^{19} atom/cm³.

7. The method of claim 1, wherein the coating comprises a silicate glass.

8. A method of doping a single crystal semiconductor substrate, comprising:

exposing a surface of the substrate to high energy particles to pre-amorphize a layer of the crystal adjacent the surface; and

implanting the substrate with a temporary impurity atom ;

heating the substrate to cause the crystal to re-grow within the layer adjacent the surface;

either before, during, or after heating, forming a coating comprising a target dopant over the surface of the substrate; and

annealing to cause the target dopant to diffuse from the coating into the substrate.

9. The method of claim 8, wherein:

the crystal comprises a semiconductor having an interstitial form;

and

during annealing, the temporary impurity atom is a faster diffusing species relative to silicon.

10. The method of claim 8, wherein the high energy particles comprise particles selected from the group consisting of Ge, In, Sb, Si, and Ar.

11. The method of claim 8, wherein the temporary impurity atom is implanted with a dose of at least about 1×10^{14} atoms/cm².

12. The method of claim 8, wherein the temporary impurity atom is fluorine.

13. The method of claim 8, wherein after annealing 90% of the target dopant that diffuses into the substrate is located within about 50 nm of the surface.

14. The method of claim 8, wherein the target dopant is boron.

15. The method of claim 8, wherein after annealing the concentration of the target dopant within the substrate adjacent the surface is at least about 1×10^{19} atom/cm³.

16. The method of claim 8, wherein the coating comprises a silicate glass.

17. A method of forming transistors, comprising:
forming a gate layer on a substrate comprising a semiconductor crystal;
forming a poly layer over the gate layer;
forming a patterned resist over the poly layer;
etching to pattern the poly layer and the gate layer, whereby a surface of the substrate is exposed;
pre-amorphizing a first layer of the semiconductor crystal adjacent the surface;
implanting a second layer of the substrate adjacent the surface with a temporary impurity atom ;

after implanting, heating to re-grow the semiconductor crystal within the first layer;

either before or after heating, forming a target dopant layer comprising a target dopant over the surface; and

5 annealing to cause the target dopant to diffuse from the target dopant layer into the substrate.

18. The method of claim 17, further comprising:

10 except where the target dopant layer functions as a spacer layer, forming a spacer layer comprising a spacer material over the target dopant layer; and

prior to annealing, etching the target dopant layer, and optionally the spacer layer, to form spacers.

15 19. The method of claim 18, wherein the target dopant layer functions as a spacer layer.

20 20. The method of claim 17, wherein the gate layer comprises a high-k dielectric.

21. The method of claim 17, wherein the second layer adjacent the substrate surface is within the first layer.

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